Architecture ATMEL AVR

Animierte Architecture von microschematics.com

Die Animation ist in FLASH programmiert; dies wird nicht mehr unterstützt. Daher muss Flash in ein anderes Video-Format gewandelt werden:

```
for f in *.swf
do
 dump-gnash  -d 100 -1 -r 1 -j 800 -k 600 --screenshot 10 -D out.raw "$f"
 ffmpeg -hide_banner -r 12 -f rawvideo -pixel_format rgb32 -video_size 800x600 -
i out.raw $f.mp4
```

(excerpt datasheet ATMEL AVR 90s8515)

- Register File 32 x 8bit
  - X, Y, Z 16bit pointer to SRAM
  - Z 16bit pointer to FLASH
- Memory address mode for REGISTERS, IO, SRAM (LDS r1, 0x13 ; load from SRAM)
  Registers are addressed like ordinary general purpose SRAM
- IO MEMORY: 64 addresses for CPU peripheral functions (control registers, timers ...)
  addressed by Register Name or SRAM Address
- in system programmable 4k x **16bit** FLASH (16bit/32bit instructions!)
  1000 write/erase cycles
- 512 byte general purpose SRAM
- STACK (16bit)
  - located in general purpose SRAM
  - stack size limited by usage of SRAM
  - user must initialize the 16bit stackpointer SP (SPH/SPL)
  - starts at top of SRAM and is decremented
- Harvard Architecture (separate memories and busses for DATA and PROGRAM)
- 2 stage pipeline (instruction is executed while the next instruction is fetched from program memory); one instruction per clock cycle

Addressing modes

1. direct single register (inc r16)
2. direct two registers (add r16,r17)
3. direct io (out PORTB, r17)
4. direct data (lds r16, $006a)
5. indirect (ld r4, X)

6. indirect with postincrement (ld r4, X+)
7. indirect with preincrement (ld r4, -X)
8. indirect with displacement (ldd r4, Y+2)
   for Y or Z only
9. constant program (lpm)
   for Z only
10. indirect program (ijmp label)
    for Z only (PC = Z)
11. relative program (rjmp label)
    PC = PC+k+1